

IMPORTANT PRODUCT INFORMATION

READ THIS INFORMATION FIRST

Product: Programmable Controller CPU Module
IC697CPU781-HB
IC697CPU782-HB

This is the production release of the IC697 PLC CPU modules version 5.50. The purpose of this release is to support the Plug & Play VME PC, the IC697 High Speed Counter module, other new features described under New Features and Functionality, and to fix the problems listed under Problems Resolved by This Upgrade.

Table 1. Catalog Numbers

New Catalog Number	Replaces
IC697CPU781-EB	IC697CPU781C,DU, D, E, EA
IC697CPU781-GB	IC697CPU781FG, GA
IC697CPU781-HB	IC697CPU781HHA
IC697CPU782-EB	IC697CPU782C, DU, D, E, EA
IC697CPU782-GB	IC697CPU782FG, GA
IC697CPU782-HB	IC697CPU782HHA

Identification

Hardware and software identification is summarized in the following tables.

Table 2. Hardware Identification

Catalog Number	Board Identification	Board Revision
IC697CPU781-EB	CPHA1	44A729676-G01 R12 or later
IC697CPU781-GB	CPHA2	44A731786-G01 R05 or R06
IC697CPU781-HB	CPHA2	44A731786-G01 R07 or later
IC697CPU782-EB	CPHA1	44A729676-G01 R12 or later
IC697CPU782-GB	CPHA2	44A731786-G01 R05 or R06
IC697CPU782-HB	CPHA2	44A731786-G01 R07 or later

Table 3. Firmware Identification

Catalog Number	EPROM Location	EPROM Label
IC697CPU781-EB/GB/HB	U72	397-005D 5.50
	U73	397-006D 5.50
	U74	397-002F 5.50
	U75	397-001F 5.50
IC697CPU782-EB/GB/HB	U72	397-007E 5.50
	U73	397-008E 5.50
	U74	397-004G 5.50
	U75	397-003G 5.50

Packaging Note

Effective with this release, the user manual will no longer be shipped with every product. User manuals are provided as a complete set in a library with IC641 Programming Software products, are available on CD ROM, or can be ordered as individual manuals.

Update Information

Upgrade kits are available to upgrade PLC CPUs to version 5.50. Existing units can be upgraded for a charge by ordering the applicable field upgrade kit. Release 5.50 is not compatible with some older versions of the 32-bit Memory Expansion boards. If you are upgrading a CPU781 or CPU782, your upgrade will depend on the revision of Expansion Memory board you have.

1. CPUs that are using Expansion Memory boards IC697MEM731A, 731B, 733A, 733B, 735A, or 735B *must upgrade with one of the following upgrade kits* that contain a firmware upgrade *and* an Expansion Memory board.

Table 4. Upgrade Kits for CPU Firmware and Memory Expansion Boards

Upgrade Kit	For Upgrading	To
44A735564G02	IC697CPU781A through H and Expansion Memory Board	IC697CPU781-EB, GB, HB and IC697MEM731D
44A735565G02	IC697CPU781A through H and Expansion Memory Board	IC697CPU781-EB, GB, HB and IC697MEM733D
44A735566G02	IC697CPU781A through H and Expansion Memory Board	IC697CPU781-EB, GB, HB and IC697MEM735D
44A735567G02	IC697CPU782A through H and Expansion Memory Board	IC697CPU782-EB, GB, HB and IC697MEM731D
44A735568G02	IC697CPU782A through H and Expansion Memory Board	IC697CPU782-EB, GB, HB and IC697MEM733D
44A735569G02	IC697CPU782A through H and Expansion Memory Board	IC697CPU782-EB, GB, HB and IC697MEM735D

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2. If you have CPUs with Expansion Memory boards IC697MEM731C, 732A, 733C, or 735C, it is recommended that you exchange them under the full warranty exchange program (see Field Service Bulletin M-11-93-23). After exchanging the Expansion Memory Board, firmware upgrades are available as listed in Table 5.

All other versions of these Expansion Memory boards are Release 5.50 compatible. To upgrade the CPU firmware to Release 5.50, use one of the upgrade kits listed below.

Table 5. Upgrade Kits for Upgrading Only CPU Firmware

Upgrade Kit	For Upgrading	To
44A731215-G08	IC697CPU781A,B, C, DU, D, E, EA	IC697CPU781-EB
	IC697CPU781FG, GA	IC697CPU781-GB
	IC697CPU781HHA	IC697CPU781-HB
44A731217-G07	IC697CPU782A, B, C, DU, D, E, EA	IC697CPU782-EB
	IC697CPU782FG, GA	IC697CPU782-GB
	IC697CPU782HHA	IC697CPU782-HB

Documentation

The following table lists the applicable documentation for the IC697CPU781 and IC697CPU782 CPUs.

Table 6. User Documentation

Catalog Number	Data Sheet	User Manual
IC697CPU781-HB	GFK-0766A	see below
IC697CPU782-HB	GFK-0767A	see below

Read this document before installing or attempting to use the IC697CPU781-HB or IC697CPU782-HB PLC CPU Module. For more information, refer to the applicable *Programmable Controller Installation manual*, *Programming Software User's Manual*, and *Programmable Controller Reference Manual*.

Table A-1. Special Operation Notes

IC641 Compatibility

1. This release of the PLC CPU modules is compatible with the versions of IC641 programming software listed in the table below. However, version 5.01 or later is required to gain access to all of the CPU's features and functionality. To work around a compatibility problem with serial IC641 programming software, the PLC will return 3.50 as its version to all serial IC641 programming software products (WSI and Standard COM) Release 3.04 and earlier.

CPU Model	IC641 Programming Software
781	Version 3.01 or later
782	Version 3.01 or later

If Release 5.50 PLC CPU firmware is used with IC641 programming software Release 4.01 or 4.02, the PLC Sweep Control and Monitor screen (F3 F8) should **ONLY** be used to change (tune) the constant window or constant sweep time. Any other use may result in the background window time being incorrectly set to 255 milliseconds. For those IC641 programming software releases used with a Release 5.50 CPU, the configuration package must be used to set the desired sweep modes or window times.

PCM and BTM Compatibility

2. With the introduction of timing improvements and new features in Release 5.00, it is highly recommended that systems using PCMs use IC697PCM711J or later. It is also highly recommended that systems using BTMs use IC697BEM713B or later. Use of boards of an earlier revision may result in lower system performance.

Notice to Upgrade GBC Hardware

3. With the introduction of new features in CPU Release 5.00, timings with the IC66* Bus Controllers (GBCs/NBCs) have changed; this has uncovered a problem in the GBC/NBC firmware. GBCs/NBCs in expanded racks could be lost if the system is fully configured and only the main rack cycles power.

Also, in previous versions of the GBC/NBC there was a problem with input data coherency. In a system with a large CPU sweep time and a short IC66* bus scan time a problem could be seen if a device is lost. Input data could be defaulted off while the CPU is reading the data from the GBC/NBC.

It is recommended to update existing GBC/NBC hardware to IC697BEM731M or later when updating PLC CPU firmware to Release 5.50. Operation of the IC697BEM731M, in conjunction with Release 5.50 of the IC697CPU will result in a slight impact to the I/O scan time of the PLC.

Foreign VME Modules

4. IC641 programming software Release 5.00 allows foreign VME modules to be configured for five modes: BUS INTERFACE, INTERRUPT ONLY, FULL MAIL, I/O SCAN, and REDUCED MAIL. However, CPU Release 5 only supports BUS INTERFACE, FULL MAIL, and I/O SCAN modes. *The other modes should not be configured.*

Maximum PLC Sweep

5. In systems configured for IC66* Bus Redundancy a complete PLC sweep must be executed every 500 ms or less, even though it is possible to configure the watchdog timer to higher limits. This also means that resetting of the watchdog timer with Service Request #8 cannot be done indefinitely.

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PCM (to CPU) Communications Timeout

6. The PCM has a default backplane communications timeout value of 5 seconds. After the PCM has sent a request to the IC697 CPU, the PCM applies this timeout while waiting on a response back from the CPU. In most cases, the CPU will respond well within the 5 second timeout, however, in certain instances the CPU can take longer than 5 seconds to respond. *These cases are limited to LOADs and/or STOREs of program and/or configuration - especially if blocks in the program are larger than 8 KBytes. Folders containing EXE blocks (again with *.EXE files >8 KBytes) are most likely to cause problems.*

Beginning with this release (5.50) of the IC697 CPUs, the CPU is guaranteed to respond within 8 seconds. To ensure that the PCMs do not observe backplane timeouts, a file must be loaded (using *termf*) to the PCM. The file must be named *CPU.ENV* and is a binary file. The contents of this file are as follows (all values are specified in hexadecimal):

FILE OFFSET	DATA															
0000	4C	5A	01	01	00	00	00	00-00	00	00	00	01	00	00	00	LZ
0010	00	00	00	00	00	00	00	00-00	00	43	50	55	4C	49	4ECPULIN
0020	4B	2E	43	4F	44	00	2D	62-00	36	34	00	2D	74	00	32	K.COD. -b.64 .-t. 2
0030	30	30	00	00	43	50	55	4C-49	4E	4B	2E	44	43	42	00	00. CPULINK .DCB.
0040	00	4E	55	4C	4C	3A	00	4E-55	4C	4C	3A	00	4E	55	4C	.NULL:.NULL:.NUL
0050	4C	3A	00	00	00	00	00	00-00	00	00	00	00	00	00	00	L :
0060	00	00	00	00	00	00	00	00-00	00	00	00	00	00	00	00
0070	00	00	00	00	00	00	00	00-00	00	00	00	00	00	00	00

Once the binary file *CPU.ENV* (above) is created, use *termf* to load *CPU.ENV* to the PCM. Then execute a soft reset of the PCM. After executing the soft reset, the PCM's backplane communications timeout should be 10 seconds.

CAUTION

A copy of the above *CPU.ENV* file can be obtained from the Electronic Bulletin Board. *CPU.ENV* can be found in the *conference:library* of *PLC:PCM* and is named *CPU.ENV*.

The *CPU.ENV* file *will not* be used when a hard reset is performed on the PCM. With the *CPU.ENV* file resident in the PCM, a soft reset must be performed after every hard reset of the PCM. Be aware that it is possible to issue a *soft reset* *COMMREQ* from the Ladder Diagram application; therefore, the application can be modified to handle the required reset of PCMs after a power cycle of the PLC system

Serial Communications

7. The following operating restrictions exist for the Serial Communications feature:
 1. Serial communications can add up to 5 ms of time to any given sweep. This should be taken into account when setting the watchdog timer.
 2. The following procedure is recommended when changing baud rates in the PLC and the WSI board. First enter the configuration package and change the baud rate on the PLC, then store the new config-

uration. Now power off the PLC and then go to the WSI setup screen and change the WSI baud rate. Finally, power the PLC back on.

3. The link idle time setting in IC641 programming software *Config for Serial Communications* should be set to 10 seconds or greater. Otherwise a communications failure will occur when storing the config to the PLC.

Serial Port Mode Configuration

8. There is a serial port configuration parameter under software configuration for the PLC called **MODE**. This configuration parameter can be one of two values: **SNP** to indicate that the serial port will be used for SNP communications, or **MSG** to indicate that the serial port will be used to send printf commands from a C program block to the connected device. If you have configured **MODE** to be **MSG** and are also using serial IC641 programming software as a means of communicating with the PLC, communications with IC641 programming software is lost when going to the RUN mode, since the serial port is currently configured for printf commands from C program blocks.

IC641/WSI Attach

9. Do not connect or disconnect the WSI/BTM cable while the programmer host is powered-on. This action may cause a running PLC to Stop.

Expansion Rack ID

10. The expansion racks for the IC697 PLC are shipped with the rack ID strapped for rack 0 (the main rack). If the rack jumper is not changed the PLC will not recognize the rack at all and may not properly identify the error.

Expansion Rack Cable

11. Do not connect or disconnect the expansion rack cable while the CPU is running. This will cause the PLC to go to the STOP/HALT mode.

Expansion Rack Power

12. Expansion racks should be powered up at the same time that the main rack is powered up, or they should be powered up after the main rack has completed its power-up initialization. *Do not power-up an expansion rack while the CPU is running power-up diagnostics.*

Memory Usage

13. A general rule-of-thumb for memory usage is 48 bytes per I/O point plus register memory in bytes.

Timer Operation

14. Care should be taken when timers (ONDTR, TMR, and OFDTR) are used in program blocks that are NOT called every sweep. The timers accumulate time across calls to the sub-block unless they are reset. This means that they function like timers operating in a program with a much slower sweep than the timers in the main program block. For program blocks that are inactive for large periods of time, the timers should be programmed in such a manner as to account for this catch up feature.

Similar to this are timers that are skipped because of the use of the JUMP instruction. Timers that are skipped will NOT catch up and will therefore not accumulate time in the same manner as if they were executed every sweep..

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I/O Link Interface

15. When powering up the PLC CPU without a battery, and I/O Link Interface boards are present, an incorrect *Loss of Module* fault will be logged for each I/O Link Interface board; but the PLC CPU will not consider these boards as lost, and the boards will continue to operate properly.

CommReqs with Retentive Memory

16. When powering up the PLC CPU with a program being retrieved from Retentive Memory and proceeding to RUN mode, any CommReqs to a PCM should be delayed for 5 seconds.

Constant Sweep

17. Constant Sweep time, when used, should be set to about 10 ms greater than the normal sweep time to avoid any oversweep conditions when monitoring or performing on-line changes with the programmer. The smallest valid constant sweep time setting is 10 milliseconds for the Model 781, 782, 914, and 924 PLCs. Window completion faults will occur if the constant sweep setting is not high enough.

Interaction of IC641 Programming Software with Closed Programming Window

18. The IC641 programming software Sweep Control and Monitor screen cannot be used to change the PLC Sweep Modes or timers (Constant Sweep Time, Program Window Times, etc.) while the program window is closed. Use Service Requests #1 through #4 to perform these functions.

Note for Using Flash Memory on CPU 781 and 782 in Conjunction With Passwords and OEM Key

19. There is a problem that can occur when using either Passwords or the OEM Key in conjunction with the Flash Memory daughterboard (IC697MEM732). This problem occurs *only* if you forget the Password or OEM Key, *and* the Flash memory has been configured to Store From Flash on power-up. If you forget the Password or OEM key, you will be unable to perform Flash operations (such as Write) from IC641 programming software, and there is no easy way to clear the Flash Memory. Since the Passwords and OEM Key are stored in Flash, they are copied to the PLC CPU on power-up along with the User Configuration and Program.

This problem is different from the case where you have forgotten the Password or OEM Key when you have a CPU with *only* battery-backed RAM (that is, Flash Memory has NOT been configured to Store From Flash on power-up). In this case, you can simply pull the board's battery, cycle power and the Passwords and OEM Key are cleared.

If you have forgotten the Password or OEM Key and the Flash Memory has been configured to Store From Flash on power-up, the corrective action is to force the Store From Flash on power-up to fail. When a Store From Flash on power-up fails, the Passwords and OEM Key are *not* copied to the PLC CPU, and Flash Operations can then be performed on the CPU. The only way to force the Store From Flash on power-up to fail is to have an incompatibility error between the PLC CPU firmware and the information stored in the Flash Memory daughterboard. In order to have an incompatibility error, the Flash Memory daughterboard must be placed on a PLC CPU motherboard that has one of the following differences:

1. *Other CPU type*: If the Flash Memory daughterboard information was created with a CPU 781, install it on a CPU 782.
2. *Earlier firmware release*: If the Flash Memory daughterboard information was created with CPU firmware Release 5.50, install it on a CPU with firmware Release 4.12 (for example).

After performing one of the above operations, the Store From Flash on power-up will fail. The Flash Memory daughterboard can now be over-written to clear the Password and OEM Key.

Error Codes When Store From Flash On Power-up Fails

20. When a Flash Memory daughterboard is configured to Store From Flash On Power-up, and the store fails, a PLC CPU Software Failure is now logged in the IC697 PLC Fault Table (Beginning with Release 5.0). The Error Code value for this failure is 95 (Hexadecimal). The first byte of the Fault Specific Data defines the reason why the Store From Flash failed. The possible values for this Fault Specific Data are as follows:

Fault Specific Data Value (Hex)	Description
CF	Specific device is not available in the system, that is, the Daughterboard is not a Flash Memory Board.
CC	Data stored on device has been corrupted and is no longer reliable. This may also occur if data in Flash memory has not been initialized.
CB	An error occurred during a read or write of the Flash Memory device
8E	Data in Flash Memory is incompatible with the PLC CPU firmware release for one of the following reasons: CPU Firmware revision Numbers Instruction Groups Supported CPU Model Number
8D	One or more specified items were not found in Flash Memory.

Using Flash Memory on CPU 781 and 782 With Changed Serial Port Parameters

21. If you change the CPU serial port characteristics (for example, data rate) and store these parameters in Flash Memory, these changes must also be made to the programming device in order to ensure successful communication with the PLC CPU the next time a serial communications link is established. If this is not done, the only way to determine the serial port settings is to interrogate the CPU from a parallel module (that is, WSI parallel IC641 programming software through a Bus Transmitter Module). The only other possibility is to initialize the Flash memory board as described in the procedure above.

General Information For Using Flash Memory on CPU 781 and 782

22. You should be aware that if the PLC is configured to Store From Flash on power-up, the current information in User RAM (User Program, Configuration, and possibly Reference Tables) **will be over-written** after the PLC is power-cycled. This may cause confusion if the program in RAM and the program in Flash Memory are different. It should also be noted that if the PLC was in RUN mode when power-cycled, it will go to RUN mode after the Store From Flash on power-up. You should exercise caution to ensure that the program and data stored during power-up is what you want to be executed by the PLC.

Caution

IC641 programming software cannot be used to change the PLC mode (STOP, RUN, etc.) while the programming window is closed. Use the toggle switch on the CPU module instead.

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Problems Resolved by This Upgrade

1. The COMM_REQ function incorrectly allowed the value of the TASK parameter to be greater than 127. When a TASK value greater than 127 is specified, an incorrect TASK value is sent to the device specified by the SYSID parameter.
2. IC697 GBC/NECs could overwrite inputs after passing data to the CPU. This would occur when a device on the IC66* bus stopped sending data but continued to send a token. Such devices are any providing global data or Field Control blocks. This problem requires companion fixes in both the IC697 CPU and the IC697 GBC/NEC. Release 5.01 of the models 788 and 789 contain the CPU fix. All GBC/NECs with catalog number IC697BEM731L, or later, have the corresponding GBC/NEC fix.
3. For function #7, the SVCREQ function block incorrectly permitted the month or day to be set to 0 when using packed ASCII format. A low bounds check is now performed and a month or day of 0 is reported as an error condition.
4. For function #17, the SVCREQ function block incorrectly required the user to specify a 0-based offset when masking/unmasking interrupts from analog input channels; this is inconsistent with masking/unmasking interrupts from discrete interrupts. Release 5.50 now requires a 1-based offset to function #17 of the SVCREQ function block when masking/unmasking interrupts from analog input channels.
5. When the CPU is powered-up, the CPU will reset all expansion rack IC697 option modules detected to be in standalone mode (PCMs). Release 5.50 does not reset these modules.
6. PSBs with input and output parameters may not have all of their data properly copied into the PSB cache memory (dependent on the bit offset and the number of bits in the parameter). This is fixed in this CPU release (Release 5.50).

New features and Functionality

Plug & Play VME PC

1. Release 5.50 of the PLC CPU together with Release 5 (or later) of IC641 programming software has the ability to provide full communications between the Plug & Play VME PC and the IC697 PLC through the VME backplane. Use of the Host Communications Toolkit (IC641SWP053) and the IC697 PLC FULL_MAIL communications driver will permit applications executing on the VME PC access to the IC697 PLC CPU, through the backplane, without the need for Ladder Diagram application support (no Absolute VME read and writes required in the user program).

IC697 High Speed Counter

2. IC697 CPU Release 5.50 and IC641 programming software Release 5.01 support the IC697 High Speed Counter (catalog number IC697HSC700).

Third Party VME I/O in CPU I/O Scan

3. Beginning with CPU Release 5.50, VME modules developed by Third Party vendors can be included in the IC697 PLC's normal I/O scan. Third Party VME modules must be designed to our specified VME interface in order to be available for inclusion in the normal PLC I/O scan. Implementation of this protocol requires execution of license GFJ-319 for each module to be integrated by a third party. Only modules that complement our offerings will be considered for inclusion under this program.

Restrictions and Open Problems

1. If an expansion rack powers up while the CPU in the main rack is in the RUN mode, the slot fault contacts will prematurely indicate that the modules in the expansion rack are not faulted *before* they complete their power up.
2. In a multi-rack system, false LOSS OF RACK faults may occur when the system loses power. If this fault is configured to be fatal, the system will power-up in STOP mode.
3. When there is no logic stored in a CPU module the %Q and %M tables will be cleared when the CPU is placed in RUN mode. In this context *no logic stored* means that no program had ever been stored or that the clear function on the IC641 programming software had been used to clear logic and configuration.
4. When the Bit Sequencer sequences from one step to another, the negative transitional contact that corresponds to the original step is not set. The transition contact for the new step is set and remains set until the sequencer sequences to the next step. This operation is identical to the operation of the previous versions of the CPU firmware.
5. If multiple faults exist in an IC697 PLC remote drop and one of them is corrected, a FAULT contact that uses the remote drop's module reference will incorrectly indicate that no faults exist at the remote drop.
6. User application faults logged for Service Request #21 can only use error codes between 0 and 2047. Use of any other error codes could cause the PLC to treat the alarms as Remote Scanner alarms.
7. An IC66* Bus Fault can set the fault condition for the M_rsbmm (r=rack, s=slot, b=bus, mm=SBA of GBC/NBC) fault and nofault contacts. This fault condition will persist until either the fault tables are cleared or the GBC's/NBC's rack is power-cycled.
8. An Analog Input Base module and its expander modules may not come online if they are configured in an expansion rack that is missing when the main rack powers up. Power-up the expansion rack first, then power-up the main rack.
9. If the main rack loses power during PLC configuration, analog input base boards (IC697ALG230) in expansion racks that do not lose power may fail. The failure would occur on the subsequent configuration. PLC configuration occurs during power up, store of configuration, and reads from Retentive (Flash) Memory. To prevent the failure, tie all racks to a common power source. To correct the failure, power-cycle the expansion racks.

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Additions to the PLC Reference Manual

The following information will be added to a future version of the *Programmable Controller Reference Manual*.

SVCREQ#5: Change Background Task Window State and Values

Use the SVCREQ function with function number 5 in order to enable or disable the background task window. The change will occur in the same CPU sweep in which the function is called.

When the window is enabled, the function returns the current time value for the window. When the window is disabled, it remains disabled until enabled again. The SVCREQ function will always pass power flow to the right for this function number.

For the Change Background Task Window function, the parameter block has a length of 1 word.

To disable the background task window, enter SVCREQ function 5 with this parameter block:

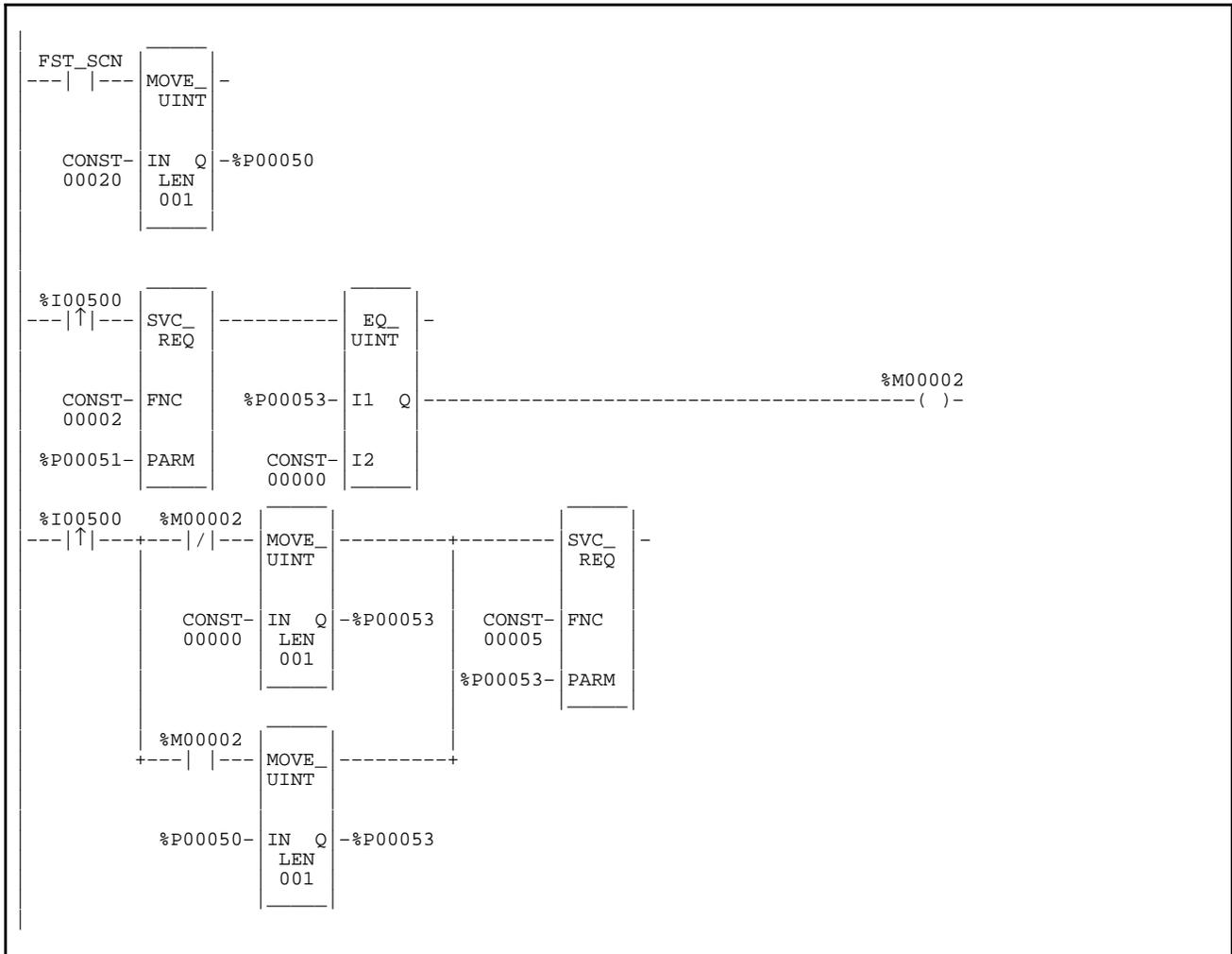
0	0	address
---	---	---------

To enable the background task window, enter SVCREQ function #5 with this parameter block:

Mode	Value from 1 to 255 ms	address
------	------------------------	---------

Example:

In the following example, when enabling contact FST_SCN is set in the first scan, the MOVE function establishes a default value of 20 ms for the background task window, using a parameter block beginning at %P00050. Later in the program when input %I00500 transitions on, the state of the background task window toggles on and off. The parameter block for all three windows is at location %P00051. Since the time for the background task window is the third value in the parameter block returned from the Read Window Values function (function #2), the location of the existing window time for the system communications window is %P00053.



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Effect of PLC Constant Sweep or Constant Window Mode on Communications Windows

When the IC697 PLC is configured for Constant Sweep or Constant Window mode, operation of the communications windows is under control of the CPU. When configured as Constant Sweep, the communications window is terminated whenever the constant sweep time is reached †

Similarly, when configured for Constant Window, the communications window is terminated whenever the constant window time is reached. If an external device is transferring a block of data, the coherency of the data block may be disrupted if the communications window terminates before completing the request. The request will complete during the next sweep; however, part of the data will have been from one sweep and the remainder will be from the following sweep.† When the communications window is in a *run to completion* mode, the data coherency problem described above does not exist.

† Constant Sweep mode can also cause the communications window to not be opened. If the Constant Sweep time is exceeded before the start of the communications window, then the communications window will not be opened during that sweep.

Sweep Impact Timing Test Results

The following tables provide Sweep Impact Times for the listed IC697 PLC CPUs. These Sweep Impact Times are the measured results of Sweep Impact Timing tests.

	781/782		914		924	
	With Point Faults Disabled (μs)	With Point Faults Enabled (μs)	With Point Faults Disabled (μs)	With Point Faults Enabled (μs)	With Point Faults Disabled (μs)	With Point Faults Enabled (μs)
Base Sweep Time	839.8	839.8	253.6	253.6	187.0	187.0
Rack Setup per expansion rack	1.0		0.5		0.5	-
I/O Scan Overhead	188.5	192.1	148.5	151.8	148.0	148.9
Per Discrete I/O module in main rack	20.9	37.0	10.5	15.4	9.0	13.6
Per Discrete I/O module in expansion rack	21.5	45.1	12.7	18.6	11.0	18.8
Per Discrete Fault		463.3		138.1		118.5
Per Analog I/O module in main rack	28.9	38.4	17.7	22.7	15.6	20.3
Per Analog I/O module in expansion rack	46.1	70.7	33.9	50.4	34.0	47.6
Per Analog Input Expander module - main rack, same segment	19.1	27.9	18.1	27.0	15.2	25.7
Per Analog Input Expander module - expansion rack, same segment	58.2	87.1	57.4	85.6	56.3	82.4
Per Analog Input Expander module - main rack, new segment	34.2	53.6	23.7	34.0	18.9	29.4
Per Analog Input Expander Module - expansion rack, new segment	71.7	106.2	60.8	91.4	59.4	88.9
Per Analog Fault	929.0		347.1		261.9	
GBC/NBC Open System Communications Window	215.3		73.6		59.0	
Per GBC/NBC polling for BackgroundMessages	22.0		7.1		6.2	
Per GBC/NBC I/O Scan	715.6		572.3		440.6	
IC66* I/O Block per I/O block scan segment	41.4	76.8	18.9	33.5	11.6	29.9
IC66* I/O block per byte discrete I/O data main rack	2.0	2.9	2.0	2.9	1.7	2.9
IC66* I/O block per byte discrete I/O data expansion rack	3.9	7.6	3.9	7.6	3.9	7.6
IC66* I/O block per word analog I/O data main rack	2.4	3.5	2.1	3.3	2.1	3.3
IC66* I/O block per word analog I/O data expansion rack	7.2	10.8	6.8	10.6	5.3	10.6
I/O Interrupt Minimum response Time	800.0		600.0		600.0	
I/O Interrupt Typical Response Time	1000.0		700.0		700.0	
I/O Interrupt Maximum Response Time	1582.1		793.0		785.0	
LAN module I/O Scan Time	40.0		23.0		23.0	
PLC Memory Access from IOMs – Read/Write 1 to 3 words	1142.2		446.5		391.9	
PLC Memory Access from IOMs – Read/Write 4 to 128 words	1278.2		572.5		495.2	
PLC Memory Access from IOMs – Read/Write each additional 128 words	1745.8		747.5		657.2	
Clock Refresh Rate	339.7		148.6		146.2	

* IC660 or IC661 products.