June 15, 1995
GFK-0770K

IMPORTANT PRODUCT INFORMATION

READ THIS INFORMATION FIRST

Product: **PLC CPU Modules**
IC697CPU781-HC
IC697CPU782-HC

This is the production release of the IC697 PLC CPU modules version 6.00. The purpose of this release is to support FIP I/O via the IC697 FIP Bus Controller, provide enhanced C programming capabilities, provide debugging of C applications running in the PLC CPU, other new features described under New Features and Functionality, and to fix the problems listed under Problems Resolved by This Upgrade.

This release is the initial offering of the IC697CPM915 and IC697CPM925 CPUs, with each providing 1 Megabyte of use logic memory.

Release 6.00 is not available for the following IC697 CPUs: IC697CPU731, 732, 771, 772, 788, 789, and 780.

Table 1. Catalog Numbers

New Catalog Number	Replaces
IC697CPU781-EC*	IC697CPU781C,DU, D, E, EA, EB
IC697CPU781-GC*	IC697CPU781F, G, GA, GB
IC697CPU781-HC	IC697CPU781H, HA, HB
IC697CPU782-EC*	IC697CPU782C, DU, D, E, EA, EB
IC697CPU782-GC*	IC697CPU782F, G, GA, GB
IC697CPU782-HC	IC697CPU782H, HA, HB

* available as field update only.

Identification

Hardware and software identification is summarized in the following tables.

Table 2. Hardware Identification

Catalog Number	Board Identification	Board Revision
IC697CPU781-EC*	CPHA1	44A729676-G01 R12 or later
IC697CPU781-GC*	CPHA2	44A731786-G01 R05 or R06
IC697CPU781-HC	CPHA2	44A731786-G01 R07 or later
IC697CPU782-EC*	CPHA1	44A729676-G01 R12 or later
IC697CPU782-GC*	CPHA2	44A731786-G01 R05 or R06
IC697CPU782-HC	CPHA2	44A731786-G01 R07 or later

* available as field update only.

Table 3. Firmware Identification

Catalog Number	EPROM Location	EPROM Label
IC697CPU781-EC*/GC*/HC	U72 U73 U74 U75	397-005E 6.00 397-006E 6.00 397-002G 6.00 397-001G 6.00
IC697CPU782-EC*/GC*/HC	U72 U73 U74 U75	397-007F 6.00 397-008F 6.00 397-004H 6.00 397-003H 6.00

* available as field update only.

Packaging Note

The user manual is not shipped with every product. User manuals are provided as a complete set in a library with IC641 Programming Software products, are available on CD-ROM, or can be ordered as individual manuals.

Update Information

Upgrade kits are available to upgrade PLC CPUs to version 6.00. Existing units can be upgraded for a charge by ordering the applicable field upgrade kit. Release 6.00 is not compatible with some older versions of the 32-bit Memory Expansion boards. If you are upgrading a CPU781 or CPU782, your upgrade will depend on the revision of Expansion Memory board you have.

1. CPUs that are using Expansion Memory boards IC697MEM731A, 731B, 733A, 733B, 735A, or 735B *must upgrade with one of the following upgrade kits* that contain a firmware upgrade *and* an Expansion Memory board.

Table 4. Upgrade Kits for CPU Firmware and Memory Expansion Boards

Upgrade Kit	For Upgrading	To
44A735564-G03	IC697CPU781A through H and Expansion Memory Board	IC697CPU781-EC, GC, HC and IC697MEM731D
44A735565-G03	IC697CPU781A through H and Expansion Memory Board	IC697CPU781-EC, GC, HC and IC697MEM733D
44A735566-G03	IC697CPU781A through H and Expansion Memory Board	IC697CPU781-EC, GC, HC and IC697MEM735D
44A735567-G03	IC697CPU782A through H and Expansion Memory Board	IC697CPU782-EC, GC, HC and IC697MEM731D
44A735568-G03	IC697CPU782A through H and Expansion Memory Board	IC697CPU782-EC, GC, HC and IC697MEM733D
44A735569-G03	IC697CPU782A through H and Expansion Memory Board	IC697CPU782-EC, GC, HC and IC697MEM735D

2. If you have CPUs with Expansion Memory boards IC697MEM731C, 732A, 733C, or 735C, it is recommended that you exchange them under the full warranty exchange program (see Field Service Bulletin M-11-93-23). After exchanging the Expansion Memory Board, firmware upgrades are available as listed in the following table.

   All other versions of these Expansion Memory boards are Release 6.00 compatible. To upgrade the CPU firmware to Release 6.00, use one of the upgrade kits listed below.

Table 5. Upgrade Kits for Upgrading Only CPU Firmware

Upgrade Kit	For Upgrading	To
44A731215-G09	IC697CPU781A, B, C, DU, D, E, EA, EB	IC697CPU781-EC
	IC697CPU781F, G, GA, GB	IC697CPU781-GC
	IC697CPU781H, HA, HB	IC697CPU781-HC
44A731217-G08	IC697CPU782A, B, C, DU, D, E, EA, EB	IC697CPU782-EC
	IC697CPU782F, G, GA, GB	IC697CPU782-GC
	IC697CPU782H, HA, HB	IC697CPU782-HC

Documentation

The following table lists the applicable documentation for the IC697CPU781 and IC697CPU782 CPUs.

Table 6. User Documentation

Catalog Number	Data Sheet	User Manual
IC697CPU781-HC	GFK-0766A, or later	see below
IC697CPU782-HC	GFK-0767A, or later	see below

Full Documentation Sets

Full documentation sets are also available in either printed/bound form or in electronic form (CD-ROM). Please refer to the following table for ordering information for full documentation sets.

Table 7. Full Documentation Set

Catalog Number	Description
IC697LBR701E	Paper library - full set of printed manuals
IC690CDR002C	CD-ROM - full set of manuals in electronic format

Read this document before installing or attempting to use the IC697CPU781-HC or IC697CPU782-HC PLC CPU Module. For more information, refer to the applicable *Programmable Controller Installation manual*, *Programming Software User's Manual*, and *Programmable Controller Reference Manual*.

Special Operation Notes

IC641 Compatibility

1. This release of the PLC CPU modules is compatible with the versions of IC641 programming software listed in the table below. However, version 6.00 or later is required to gain access to all of the CPU's features and functionality. To work around a compatibility problem with serial IC641 programming software, the PLC will return 3.60 as its version to all serial IC641 programming software products (WSI and Standard COM) Release 3.04 and earlier.

CPU Model	IC641 Programming Software
781	Version 3.01 or later
782	Version 3.01 or later

If Release 6.00 PLC CPU firmware is used with IC641 programming software Release 4.01 or 4.02, the PLC Sweep Control and Monitor screen (F3 F8) should **ONLY** be used to change (tune) the constant window or constant sweep time. Any other use may result in the background window time being incorrectly set to 255 milliseconds. For those IC641 programming software releases used with a Release 6.00 CPU, the configuration package must be used to set the desired sweep modes or window times.

Microcycle Mode and First Output Scan

2. Microcycle mode is a new sweep mode of the release 6.00 CPU. In this mode, the PLC keeps the time interval between I/O scans constant (for a further description of Microcycle mode see *New Features and Functionality*) – actually the start of sweep time is maintained as a fixed interval.

   In keeping the time interval between I/O scans constant, the CPU must know the amount of the sweep to be allocated to the output scan. Under normal operating situations, the amount of time required to complete the previous sweep's output scan is used to estimate the amount of time required to complete this sweep's output scan.

   Obviously, this manner of estimating the amount of time required for the output scan does not work for the first output scan of the IC697 PLC. Since no previous sweep's output scan time is available, the release 6.00 CPU will estimate the output scan time based upon the configured base cycle time. The first output scan will be estimated as one-third of the configured base cycle time. (e.g., if the base cycle time is configured to be 60 ms, then the first output scan will be estimated as requiring 20 ms). When programming for first scan, ensure that the logic to be performed in a given program will complete prior to the next execution time for that same program.

PCM and BTM Compatibility

3. With the introduction of timing improvements and new features in Release 5.00, it is highly recommended that systems using PCMs use IC697PCM711J or later. It is also highly recommended that systems using BTMs use IC697BEM713B or later. Use of boards of an earlier revision may result in lower system performance.

PCM (to CPU) Communications Timeout

4. The PCM has a default backplane communications timeout value of 5 seconds. After the PCM has sent a request to the IC697 CPU, the PCM applies this timeout while waiting on a response back from the CPU. In most cases, the CPU will respond well within the 5 second timeout, however, in certain instances the CPU can take longer than 5 seconds to respond. *These cases are limited to LOADs and/or STOREs of program and/or configuration - especially if blocks in the program are larger than 8 KBytes. Folders containing EXE blocks (again with *.EXE files >8 KBytes) are most likely to cause problems. Beginning in Release 6.00 Standalone C programs larger than 8 Kbytes also cause this to happen.*

   Beginning in release (5.50) of the IC697 CPUs, the CPU is guaranteed to respond within 8 seconds. To ensure that the PCMs do not observe backplane timeouts, a file must be loaded (using *termf*) to the PCM. The file must be named *CPU.ENV* and is a binary file. The contents of this file are as follows (all values are specified in hexadecimal):

FILE OFFSET	DATA															
0000	4C	5A	01	01	00	00	00	00-00	00	00	00	01	00	00	00	LZ . . . . .
0010	00	00	00	00	00	00	00	00-00	00	43	50	55	4C	49	4E	. . . . . CPULIN
0020	4B	2E	43	4F	44	00	2D	62-00	36	34	00	2D	74	00	32	K . C O D . –b . 6 4 . –t . 2
0030	30	30	00	00	43	50	55	4C-49	4E	4B	2E	44	43	42	00	0 0 . .C P U L I NK . D C B .
0040	00	4E	55	4C	4C	3A	00	4E-55	4C	4C	3A	00	4E	55	4C	. N U L L: . N U L L: . N U L
0050	4C	3A	00	00	00	00	00	00-00	00	00	00	00	00	00	00	L : . . . . .
0060	00	00	00	00	00	00	00	00-00	00	00	00	00	00	00	00	. . . . .
0070	00	00	00	00	00	00	00	00-00	00	00	00	00	00	00	00	. . . . .

   Once the binary file CPU.ENV (above) is created, use *termf* to load CPU.ENV to the PCM. Then execute a soft reset of the PCM. After executing the soft reset, the PCM's backplane communications timeout should be 10 seconds.

Note

A copy of the above CPU.ENV file can be obtained from the Electronic Bulletin Board Service (BBS). CPU.ENV can be found in the *conference:library* of PLC:PCM and is named *CPU.ENV.*

CAUTION

The CPU.ENV file *will not* be used when a hard reset is performed on the PCM. With the CPU.ENV file resident in the PCM, a soft reset must be performed after every hard reset of the PCM. Be aware that it is possible to issue a *soft reset* COMMREQ from the Ladder Diagram application; therefore, the application can be modified to handle the required reset of PCMs after a power cycle of the PLC system

Notice to Upgrade GBC Hardware

5. With the introduction of new features in CPU Release 5.00, timings with the IC66* Bus Controllers (GBCs / NBCs) have changed; this has uncovered a problem in the GBC / NBC firmware. GBCs / NBCs in expanded racks could be lost if the system is fully configured and only the main rack cycles power.

   Also, in previous versions of the GBC / NBC there was a problem with input data coherency. In a system with a large CPU sweep time and a short IC66* bus scan time a problem could be seen if a device is lost. Input data could be defaulted off while the CPU is reading the data from the GBC / NBC.

   It is recommended to update existing GBC/NBC hardware to IC697BEM731M or later when updating PLC CPU firmware to Release 6.00. Operation of the IC697BEM731M, in conjunction with Release 6.00 of the IC697CPU will result in a slight impact to the I/O scan time of the PLC.

Third Party VME Modules

6. IC641 programming software Release 5.00 (and later) allows Third Party VME modules to be configured for five modes: BUS INTERFACE, INTERRUPT ONLY, FULL MAIL, I/O SCAN, and REDUCED MAIL. However, CPU Release 5 only supports BUS INTERFACE, FULL MAIL, and I/O SCAN modes. *The other modes should not be configured.*

Maximum PLC Sweep

7. In systems configured for IC66* Bus Redundancy a complete PLC sweep must be executed every 500 ms or less, even though it is possible to configure the watchdog timer to higher limits. This also means that resetting of the watchdog timer with Service Request #8 cannot be done indefinitely.

Serial Communications

8. The following operating restrictions exist for the Serial Communications feature:

   1. Serial communications can add up to 5 ms of time to any given sweep. This should be taken into account when setting the watchdog timer.

   2. The following procedure is recommended when changing baud rates in the PLC and the WSI board. First enter the configuration package and change the baud rate on the PLC, then store the new configuration. Now power off the PLC and then go to the WSI setup screen and change the WSI baud rate. Finally, power the PLC back on.

   3. The link idle time setting in IC641 programming software *Config for Serial Communications* should be set to 10 seconds or greater. Otherwise a communications failure will occur when storing the config to the PLC.

Serial Port Mode Configuration

9. There is a serial port configuration parameter under software configuration for the PLC called MODE. This configuration parameter can be one of two values: **SNP** to indicate that the serial port will be used for SNP

communications, or **MSG** to indicate that the serial port will be used to send printf commands from a C program block to the connected device. If you have configured MODE to be **MSG** and are also using serial IC641 programming software as a means of communicating with the PLC, communications with IC641 programming software is lost when going to the RUN mode, since the serial port is currently configured for printf commands from C program blocks.

IC641/WSI Attach

10. Do not connect or disconnect the WSI/BTM cable while the programmer host is powered-on. This action may cause a running PLC to Stop.

Expansion Rack ID

11. The expansion racks for the IC697 PLC are shipped with the rack ID strapped for rack 0 (the main rack). If the rack jumper is not changed the PLC will not recognize the rack at all and may not properly identify the error.

Expansion Rack Cable

12. Do not connect or disconnect the expansion rack cable while the CPU is running. This will cause the PLC to go to the STOP/HALT mode.

Expansion Rack Power

13. Expansion racks should be powered up at the same time that the main rack is powered up, or they should be powered up after the main rack has completed its power-up initialization. *Do not power-up an expansion rack while the CPU is running power-up diagnostics.*

Memory Usage

14. A general rule-of-thumb for memory usage is 48 bytes per I/O point plus register memory in bytes.

Timer Operation

15. Care should be taken when timers (ONDTR, TMR, and OFDTR) are used in program blocks that are NOT called every sweep. The timers accumulate time across calls to the sub-block unless they are reset. This means that they function like timers operating in a program with a much slower sweep than the timers in the main program block. For program blocks that are inactive for large periods of time, the timers should be programmed in such a manner as to account for this catch up feature.

    Similar to this are timers that are skipped because of the use of the JUMP instruction. Timers that are skipped will NOT catch up and will therefore not accumulate time in the same manner as if they were executed every sweep..

I/O Link Interface

16. When powering up the PLC CPU without a battery, and I/O Link Interface boards are present, an incorrect *Loss of Module* fault will be logged for each I/O Link Inter-

face board; but the PLC CPU will not consider these boards as lost, and the boards will continue to operate properly.

CommReqs with Retentive Memory

17. When powering up the PLC CPU with a program being retrieved from Retentive Memory and proceeding to RUN mode, any CommReqs to a PCM should be delayed for 5 seconds.

Constant Sweep

18. Constant Sweep time, when used, should be set to about 10 ms greater than the normal sweep time to avoid any oversweep conditions when monitoring or performing on-line changes with the programmer. The smallest valid constant sweep time setting is 10 milliseconds for the Model 781, 782, 914, 915, 924, and 925 PLCs. Window completion faults will occur if the constant sweep setting is not high enough.

Interaction of IC641 Programming Software with Closed Programming Window

19. The IC641 programming software Sweep Control and Monitor screen cannot be used to change the PLC Sweep Modes or timers (Constant Sweep Time, Program Window Times, etc.) while the program window is closed. Use Service Requests #1 through #4 to perform these functions.

Note for Using Flash Memory on CPU 781 and 782 in Conjunction With Passwords and OEM Key

20. A problem that can occur when using either Passwords or the OEM Key in conjunction with the Flash Memory daughterboard (IC697MEM732). This problem occurs *only* if you forget the Password or OEM Key, *and* the Flash memory has been configured to Store From Flash on power-up. If you forget the Password or OEM key, you will be unable to perform Flash operations (such as Write) from IC641 programming software, and there is no easy way to clear the Flash Memory. Since the Passwords and OEM Key are stored in Flash, they are copied to the PLC CPU on power-up along with the User Configuration and Program.

    This problem is different from the case where you have forgotten the Password or OEM Key when you have a CPU with *only* battery-backed RAM (that is, Flash Memory has NOT been configured to Store From Flash on power-up). In this case, you can simply pull the board's battery, cycle power and the Passwords and OEM Key are cleared.

    If you have forgotten the Password or OEM Key and the Flash Memory has been configured to Store From Flash on power–up, the corrective action is to force the Store From Flash on power-up to fail. When a Store From Flash on power-up fails, the Passwords and OEM Key are *not* copied to the PLC CPU, and Flash Operations can then be performed on the CPU. The only way to force the Store From Flash on power-up to fail is to have an incompatibility error between the PLC CPU firmware and the information stored in the Flash Memory daughterboard. In order to have an incompatibility error, the Flash Memory daughterboard must be placed on a PLC CPU motherboard that has one of the following differences:

1. *Other CPU type*: If the Flash Memory daughterboard information was created with a CPU 781, install it on a CPU 782.
2. *Earlier firmware release*: If the Flash Memory daughterboard information was created with CPU firmware Release 6.00, install it on a CPU with firmware Release 4.12 (for example).

After performing one of the above operations, the Store From Flash on power-up will fail. The Flash Memory daughterboard can now be over-written to clear the Password and OEM Key.

Error Codes When Store From Flash On Power-up Fails

21. When a Flash Memory daughterboard is configured to Store From Flash On Power-up, and the store fails, a PLC CPU Software Failure is now logged in the IC697 PLC Fault Table (Beginning with Release 5.00). The Error Code value for this failure is 95 (Hexadecimal). The first byte of the Fault Specific Data defines the reason why the Store From Flash failed. The possible values for this Fault Specific Data are as follows:

Fault Specific Data Value (Hex)	Description
CF	Specific device is not available in the system, that is, the Daughterboard is not a Flash Memory Board.
CC	Data stored on device has been corrupted and is no longer reliable. This may also occur if data in Flash memory has not been initialized.
CB	An error occurred during a read or write of the Flash Memory device
8E	Data in Flash Memory is incompatible with the PLC CPU firmware release for one of the following reasons: CPU Firmware revision Numbers Instruction Groups Supported CPU Model Number
8D	One or more specified items were not found in Flash Memory.

Using Flash Memory on CPU 781 and 782 With Changed Serial Port Parameters

22. If you change the CPU serial port characteristics (for example, data rate) and store these parameters in Flash Memory, these changes must also be made to the programming device in order to ensure successful communication with the PLC CPU the next time a serial communications link is established. If this is not done, the only way to determine the serial port settings is to interrogate the CPU from a parallel module (that is, WSI parallel IC641 programming software through a Bus Transmitter Module). The only other possibility is to initialize the Flash memory board as described in the procedure above.

General Information For Using Flash Memory on CPU 781 and 782

23. You should be aware that if the PLC is configured to Store From Flash on power-up, the current information in User RAM (User Program, Configuration, and possibly Reference Tables) ***will be over-written*** after the PLC is power-cycled. This may cause confusion if the program in RAM and the program in Flash Memory are different. It should also be noted that if the PLC was in RUN mode when power-cycled, it will go to RUN mode after the Store From Flash on power-up. You should exercise caution to ensure that the program and data stored during power-up is what you want to be executed by the PLC.

Caution

IC641 programming software cannot be used to change the PLC mode (STOP, RUN, etc.) while the programming window is closed. Use the toggle switch on the CPU module instead.

Problems Resolved by This Upgrade

1. The Service Request function block, when processing request #20 took an exceptionally long time to complete (10+ milliseconds).
2. Occasionally the CPU would not perform its full power-up diagnostic checks even when powering-up into STOP mode.
3. The Service Request function block function code #21 incorrectly permitted use of error codes greater than 800h. Such error codes were interpreted by the PLC CPU as being Remote Scanner alarms.
4. An IC66* bus fault could have set the fault condition for the M_rsbmm (r=rack, s=slot, b=bus, mm=SBA of GBC/NBC) fault and no fault contacts. This fault condition persisted until either the fault tables were cleared or the GBC's/NBC's rack was power-cycled.
5. Expansion rack Analog Input Expander cards were reset (LED out) during a run mode reconfiguration.
6. The CPU rack is powered off and an expansion rack containing a PCM is powered up. The PCM is given sufficient time to complete its self tests then times out the CPU and proceeds into PCM standalone mode. If the CPU is then powered up, the PCM is not reset but no indication is given to the user that the PCM is not configured.
7. The CPU did not verify that interrupt trigger declarations in the program correctly corresponded to interrupt generating modules declared in the I/O configuration.
8. The Time of Day clock incorrectly handled leap year.
9. Attempting to read (from an external device) the %L memory associated with an EXE block resulted in the CPU LEDs going out. A subsequent power-up showed a PLC CPU Software Fault (error code 8Dh) in the PLC fault table.
10. When using SVCREQ function #20 to read the PLC or I/O fault tables, occasionally the header information returned and the current state of the fault tables was inconsistent.
11. Pre-release 6.00 CPUs occasionally do not always work with new GE Fanuc power supplies. Problems may be observed when using PWR710E, PWR710F, and PWR724A. The symptoms are typically a loss of option module(s) in expansion rack(s).

New features and Functionality

Standalone C Program

1. IC697 CPU release 6.00 now provides the ability to have PLC CPU application written exclusively in the C language. A standalone C program is called from the operating system directly – no Ladder Logic is required. Each standalone C program (code and data) can be a maximum of 512 Kbytes, providing there is sufficient RAM available on the PLC CPU.

   A standalone C program can have up to eight input specifications and up to eight output specifications. Each input or output specification is defined as a start PLC memory reference and a data length. The input specifications are copied into the standalone C program when the standalone is scheduled for execution by the operating system. Output specifications are copied back to the specified PLC global memory upon completion of the standalone C program's execution. Each of the input / output specifications are defined by the user through IC641 programming software release 6.00.

   Standalone C programs are created using the C Programmer's Toolkit for IC697 PLCs (v3.00). For more information on Standalone C programs, please consult the *Programmable Controller Reference Manual* or *C Programmer's Toolkit for PLCs User's Manual.*

Multiple Programs

2. Release 6.00 of the IC697 PLC CPU now supports the storing of multiple programs to a single PLC. A maximum of 16 programs can be store to the release 6.00 IC697 CPU. Of the 16, only one can be a Ladder Logic / SFC program. Therefore a release 6.00 PLC CPU can take a maximum of one LD / SFC program and 15 Standalone C programs *OR* 16 Standalone C programs. The PLC CPU must still contain sufficient available User RAM to store all programs.

Embedded Debugger for C Applications

3. The IC697 CPU, beginning with release 6.00, now includes a C debugger embedded in the CPU firmware. The embedded debugger is for use in debugging C applications running in the IC697 PLC CPU. Some of the capabilities provided by the embedded debugger include the setting of hardware and / or software breakpoints, establishing watch variables, display / edit C application data, single step execution of the C application, and step-over / step-intoexecution control. The embedded debugger may be used to debug C (EXE) blocks and Standalone C programs in the release 6.00 IC697 PLC CPU. Only one debug session is permitted at any time. When debugging a C application, start / stop control of the program is controlled through the embedded debugger, however, the IC697 PLC continues to execute its sweep – executing any other program in the CPU, scanning I / O, communicating with IC641 programming software (if connected), and communicating with any option modules (if present). A new C Toolkit, the PLC C Toolkit Professional (IC641SWP719A), is required to use the embedded debugger. The new C Toolkit provides the User Interface program for controlling the embedded debugger and the required communications drivers. Communications between the User Interface and the IC697 CPU is via SNP on the CPU's built-in serial port. (Note: Debugger communications drivers and User Interface program are DOS–based applications)

FIP I/O

4. The release 6.00 IC697 CPU now supports FIP I/O (a new type of I/O network) and the FIP Bus Controller (FBC). For more information on FIP I/O and the FIP Bus Controller please refer to the *FIP Bus Controller User's Manual*.

Microcycle Sweep Mode

5. Microcycle is a new Sweep Mode of the release 6.00 IC697 PLC CPU. In microcycle mode, each sweep begins at an absolute time relative to the STOP-to-RUN transition time. Programs are configured by the user to run at whole number intervals of the base cycle time. In microcycle mode the overall sweep is much like that of Constant Sweep, however, program execution can be *time sliced* over several sweeps. Higher priority (must run often) programs are given smaller intervals of the base cycle time, whereas lower priority (run less often) programs are given larger intervals. The interval defines how often the program will be scheduled for execution (e.g., an interval of 1 indicates that this program must execute every sweep. An interval of 3 indicates that the program should be scheduled for execution every third sweep.) Programs with interval 1 must be scheduled and complete execution every sweep. Programs with intervals greater than 1 are scheduled based on their interval, but execution of any given program need only complete prior to its next interval time to be scheduled. A program with interval 2 does not necessarily run 1/2 the program in one sweep and 1/2 in the next, and a program with interval 3 does not necessarily run 1/3 of its execution across 3 sweeps.

Note

The prior execution of a given program must complete before that same program can be scheduled for its next execution. If the program did not complete its prior execution, then at the time is to be scheduled, a fault will be logged and the program will not be scheduled on this interval.

Multiple SNP Sessions

6. The Release 6.00 IV697 PLC CPU now supports multiple logical connections through the CPU's built-in serial port. This functionality is provided in conjunction with the Host Communications Toolkits to permit multiple user applications running in the same host computer to communicate serially (SNP) with the IC697 CPU via the Host Communications Toolkits and an SNP driver.

One Megabyte User Logic Memory

7. Beginning with IC697 PLC CPU release 6.00, two new CPU models will be available: CPM915 and CPM925. Both of these models provide 1 Megabyte (1024 kilobytes) of User Logic memory. These CPUs support multiple programs with the restrictions that no single program can be larger than 512 Kbytes and only one LD/SFC program is permitted. IC641 programming software Release 6.00 is required to configure these new CPU models.

CPM915 and CPM925

8. These are two new IC697 PLC CPU models with each providing 1 megabyte of user logic memory. (Please refer to above discussion of new 1 Megabyte User Logic Memory option for details.)

FIP Device Status References (F_rsnnn)

9. With the addition of FIP I/O to the release 6.00 IC697 CPU, we have included FIP device status references. These FIP device status references are analogous to the Module status references provided for use with GENIUS bus based devices (M_rsbmm). FIP device status references take the form:

   F_rsnnn

   where: **F** indicates this is a FIP device status reference
   r indicates the VME rack number of the FIP Bus Controller
   s indicates the VME slot number of the FIP Bus Controller
   nnn indicates the node id of the FIP I/O nest

   The FIP device status references are to be used with the FAULT and NOFLT contacts to determine if an I/O nest on the FIP I/O network has a fault condition.

Interrupt Blocks Calling Other Blocks

10. Previous releases of the IC697 PLC CPU have not permitted calls to other blocks from within an LD block configured as an I/O or Timed Interrupt Block. This restriction has been removed with release 6.00.

14-Point Interrupt Module

11. Support for the IC697 14-point Interrupt Module has been incorporated into the release 6.00 IC697 PLC CPU. Use of the 14-point Interrupt Module with prior versions of the IC697 PLC CPU required application support from within the user's logic program to interface with and control the 14-point Interrupt module. This support is now in the CPU firmware.

Note

When upgrading to IC697 CPU release 6.00, the PLC logic associated with supporting the 14-point Interrupt Module ***MUST*** be removed from the application program prior to placing the release 6.00 CPU into RUN mode. If this support logic is not removed, incorrect operation of the 14-point Interrupt Module, the application program, and the IC697 PLC CPU firmware will result.

Restrictions and Open Problems

1. If multiple faults exist in an IC697 PLC remote drop and one of them is corrected, a FAULT contact that uses the remote drop's module reference will incorrectly indicate that no faults exist at the remote drop.

2. An Analog Input Base module and its expander modules may not come online if they are configured in an expansion rack that is missing when the main rack powers up. Power-up the expansion rack first, then power-up the main rack.

3. If the main rack loses power during PLC configuration, analog input base boards (IC697ALG230) in expansion racks that do not lose power may fail. The failure would occur on the subsequent configuration. PLC configuration occurs during power up, store of configuration, and reads from Retentive (Flash) Memory. To prevent the failure, tie all racks to a common power source. To correct the failure, power-cycle the expansion racks.

4. If an expansion rack powers up while the CPU in the main rack is in the RUN mode, the slot fault contacts will prematurely indicate that the modules in the expansion rack are not faulted *before* they complete their power up.

5. In a multi-rack system, false LOSS OF RACK faults may occur when the system loses power. If this fault is configured to be fatal, the system will power-up in STOP mode.

6. When there is no logic stored in a CPU module the %Q and %M tables will be cleared when the CPU is placed in RUN mode. In this context *no logic stored* means that no program had ever been stored or that the clear function on the IC641 programming software had been used to clear logic and configuration.

7. When the Bit Sequencer sequences from one step to another, the negative transitional contact that corresponds to the original step is not set. The transition contact for the new step is set and remains set until the sequencer sequences to the next step. This operation is identical to the operation of the previous versions of the CPU firmware.

8. The CPU will erroneously report that it is still in STOP / IOSCAN mode even after clearing configuration if the CPU was in STOP / IOSCAN prior to the config clear. (Presence / absence of Program and / or clearing of program does not affect this situation). NOTE: the CPU will **NOT** scan any I / O under these circumstances. Once the Configuration is cleared, the CPU suspends I / O scanning. Only the indication of *STOP/IOSCAN* to the user is incorrect.

9. If the CPU is to power-up into RUN mode the full power-up diagnostic tests are supposed to be skipped. If *only* an I / O configuration (no program) is stored to the PLC and the PLC is placed in RUN mode, then a power-cycle of the PLC will result in the CPU performing its full power-up diagnostic tests.

Additions to the PLC Reference Manual

IC697 Instruction Set: SVCREQ #15

Page 4-214 of the G version of the *Programmable Logic Controller Reference Manual* provides a description of the returned data when a SVCREQ #15 is executed (read last fault). The number of bytes of meaningful fault specific data varies depending on whether the logged fault is long or short and also whether it is an I/O fault or a PLC fault.

Referring to the fault table descriptions on page 4-213 and 4-214, the Long/Short indicator (in the least significant byte of word address + 1) defines the number of bytes of meaningful fault specific data present in the fault memory. Defined values are:

Fault Table Type	Long/Short Value
PLC Fault Table	00 = 8 bytes (short)
	01 = 24 bytes (long)
I/O Fault Table	02 = 5 bytes (short)
	03 = 21 bytes (long)

IC697 Instruction Timing

Table A-1 below contains updated information for several of the IC697 CPU instruction timings. These updates apply to those numbers given in the *Programmable Controller Reference Manual*, in appendix A.

Table A-1. Instruction Timing

Function Group	Function	Enabled				Disabled				Increment				Size
		924/925	914/915	781/782	731/732 771/772	924/925	914/915	781/782	731/732 771/772	924/925	914/915	781/782	731/732 771/772	
Relational	RANGE(INT)	9	11	33	–	3	4	12	–	–	–	–	–	18
	RANGE(DINT)	10	13	38	–	3	5	12	–	–	–	–	–	18
Bit Operation	AND (WORD)	16	19	61	116	5	7	26	35	0.5	0.5	8.0	18.0	18
	OR (WORD)	15	19	62	118	6	7	26	35	0.5	0.5	9.0	19.0	18
	XOR (WORD)	7	19	58	118	5	7	23	35	0.5	0.5	9.0	19.0	18
	NOT (WORD)	10	13	40	76	5	6	23	32	0.4	0.5	3.0	8.0	15
	NOT (DWORD)	8	12	40	79	6	7	22	31	0.1	0.5	3.0	10.0	15
	MCMP (WORD)	19	23	98	212	7	11	36	58	0.6	1.0	3.0	8.0	30
	SHL (WORD)	11	17	63	137	5	8	30	41	0.6	1.0	4.0	10.0	24
	SHR (WORD)	12	19	64	138	5	9	27	42	0.5	1.0	4.0	10.0	24
	ROL (WORD)	12	16	57	119	5	6	24	53	0.5	1.0	4.0	9.0	18
	ROR (WORD)	9	15	53	113	5	6	23	34	0.6	1.0	4.0	9.0	18
	MOVE (BIT)	13	19	58	119	5	7	20	32	0.8	1.0	3.0	6.0	15
	BPOS (WORD)	9	15	55	107	5	7	25	35	0.2	0.5	1.0	4.0	18
	BPOS (DWORD)	13	20	81	158	5	8	23	36	0.2	0.5	3.0	6.0	18
Array	ARRAY_RANGE (WORD)	13	17	53	–	4	5	14	–	0.9	1.0	1.4	–	21
	ARRAY_RANGE (DWORD)	13	18	53	–	4	5	14	–	0.9	1.0	3.9	–	21
Control	SVCREQ:									–	–	–	–	12
	#23	74	98	302	–	2	3	10	–	–	–	–	–	12
	#25	19	26	79	–	2	4	10	–	–	–	–	–	12
	#32	42	52	148	–	3	4	10	–	–	–	–	–	12

1. Time (in microseconds) is based on Release 6.0 of IC641 programming software software ("–" indicates value not available, not applicable, or not supported with release 6)
2. For table functions, increment is in units of length specified. For bit operation functions, microseconds/bit. For data move functions, microseconds/the number of bits or words.
3. Enabled time is for single length units of type %R.

Sweep Impact Timing Test Results

	CPU781/782		CPM914/915		CPM924/925	
	with Point Faults Disabled (ms)	**with Point Faults Enabled (ms)**	**with Point Faults Disabled (ms)**	**with Point Faults Enabled (ms)**	**with Point Faults Disabled (ms)**	**with Point Faults Enabled (ms)**
Base Sweep Time	702.5	702.5	207.4	207.4	152.5	152.5
Rack Setup per expansion Rack	1.0		0.5		0.5	
I/O Scan Overhead	175.6	196.9	138.2	148.0	134.8	141.2
Per Discrete I/O module in main rack	20.9	28.3	10.5	15.6	9.0	13.6
Per Discrete I/O module in expansion rack	22.6	39.8	11.0	18.3	10.2	14.9
Per Discrete Fault		425.6		157.0		118.9
Per Analog I/O module in main rack	27.9	30.8	16.0	22.3	14.9	20.7
Per Analog I/O module in expansion rack	48.0	76.1	31.8	52.3	32.1	46.4
Per Analog Input Expander in main rack in same segment	18.8	27.5	16.9	25.9	15.2	24.2
Per Analog Input Expander in same segment in expansion rack	57.0	85.6	56.7	83.6	55.8	82.4
Per Analog Input Expander in new segment in main rack	36.6	51.4	22.7	32.4	20.3	27.9
Per Analog Input Expander in new segment in expansion rack	70.5	104.7	65.3	93.4	59.8	88.3
Per Analog Fault	936.2		329.6		259.7	

	CPU781/782		CPM914/915		CPM924/925	
	with Point Faults Disabled (mѕ)	**with Point Faults Enabled (mѕ)**	**with Point Faults Disabled (mѕ)**	**with Point Faults Enabled (mѕ)**	**with Point Faults Disabled (mѕ)**	**with Point Faults Enabled (mѕ)**
GBC Open System Comm. Window	189.0		61.6		43.2	
per GBC polling for Background Messages	20.0		8.6		8.1	
per GBC I/O Scan	811.0		647.6		423.7	
Genius I/O Block per I/O block scan segment	44.4	72.5	30.0	60	27.0	54.0
Genius I/O Block per byte discrete I/O data main rack	3.1	4.3	1.7	3.4	1.5	3.0
Genius I/O Block per byte discrete I/O data exp. rack	4.5	15.3	2.5	4.0	2.0	4.2
Genius I/O Block per word analog I/O data main rack	4.2	9.1	1.1	1.6	1.1	1.6
Genius I/O Block per word analog I/O data exp. rack	13.1	16.0	5.7	9.33	4.0	6.0
FIP I/O Block per I/O block scan segment	29.0	67.0	11.6	15.3	11.4	11.9
FIP I/O Block per byte discrete I/O data main rack	2.5	4.8	2.4	2.9	1.9	2.9
FIP I/O Block per byte discrete I/O data exp. rack	4.4	6.4	2.6	3.3	2.4	2.8
FIP I/O Block per word analog I/O data main rack	7.1	8.8	1.1	1.9	0.8	1.8
FIP I/O Block per word analog I/O data exp. rack	9.8	13.1	3.2	5.8	4.3	4.9
PLC Memory Access from IOMs – Read/Write 1 to 3 words	1206		445		399	
PLC Memory Access from IOMs – Read/Write 4 to 128 words	1393		579		483	
PLC Memory Access from IOMs – Read/Write each additional 128 words	1835		803		653	
Clock Refresh Rate	324.8		145.5		138.6	
LAN module I/O Scan Time	66.5		58.6		47.1	

	CPU781/782		CPM914/915		CPM924/925	
	Block (ms)	**Program (ms)**	**Block (ms)**	**Program (ms)**	**Block (ms)**	**Program (ms)**
I/O Interrupt Minimum Response Time	675	778	359	370	313	326
I/O Interrupt Typical Response Time	679	797	363	386	316	331
I/O Interrupt Maximum Response Time	1633	1734	772	783	627	640
Timed Interrupt Minimum Response Time	227	318	147	151	108	113
Timed Interrupt Typical Response Time	346	403	185	195	143	150
Timed Interrupt Maximum Response Time	464	507	219	229	163	166